What is Claimed is:

1. A high slew rate amplifying circuit for a TFT-type of LCD system, the amplifying circuit comprising:

an operational amplifier;

a pull-up transistor connected to an output of the operational amplifier;

a pull-down transistor to the output of the operational amplifier;

a control circuit to selectively actuate the pull-up transistor and the pull-down transistor, respectively.

2. The amplifying circuit of claim 1, wherein the control circuit is operable to selectively actuate each of the pull-up and pull-down transistors, respectively, for one of the following: less than about 1/2 of the period of a polarity signal; or less than the period of an output enable signal.

3. The amplifying circuit of claim 2, wherein the control circuit is operable to selectively actuate each of the pull-up and pull-down transistors, respectively, for one of the following: less than about 1/20 period of the polarity signal; or less than about 1/10 of the period of the output enable signal.

4. The amplifying circuit of claim 3, wherein the control circuit is operable to selectively actuate each of the pull-up and pull-down transistors, respectively, for one of the following: less than about 1/200 of the period of the

polarity signal; or less than about 1/100 of the period of the output enable signal.

5. The amplifying circuit of claim 1, wherein the control circuit includes:

a first one-shot circuit to generate a first one-shot signal that determines actuation time of the pull-up transistor; and

a second one-shot rising circuit to generate a second one-shot signal that determines actuation time of the pull-down transistor.

6. The amplifying circuit of claim 5, wherein the first and second one-shot signals are determined as a function of an output enable signal.

7. The amplifying circuit of claim 5, wherein each of the first and second one-shot circuits includes at least one delay unit, respectively, to delay a transition in the respective one-shot signal relative to a transition in the output enable signal.

8. The amplifying circuit of claim 1, wherein the operational amplifier includes a high-part amplifying sub-circuit and a low-part amplifying sub-circuit.

9. The amplifying circuit of claim 8, wherein the high-part amplifying sub-circuit has voltage follower configuration including a plurality of transistors.

10. The amplifying circuit of claim 9, wherein the high-part amplifying sub-circuit further includes at least one capacitor.

11. The amplifying circuit of claim 8, wherein the low-part amplifying sub-circuit has voltage follower configuration including a plurality of transistors.

12. The amplifying circuit of claim 11, wherein the low-part amplifying sub-circuit further includes at least one capacitor.

13. The amplifying circuit of claim 8, wherein the pull-up transistor is connected to the output of the high-part amplifying sub-circuit and the pull-down transistor is connected to the output of the low-part amplifying sub-circuit.

14. The amplifying circuit of claim 8, wherein the control circuit is operable to selectively control the pull-up and pull-down transistors, respectively, based upon an output enable signal.

15. A high slew rate amplifying apparatus for a TFT-type of LCD system, the apparatus comprising:

operational amplifying means;

pull-up means for pulling up the output signal of the operational amplifying means;

pull-down means for pulling down the output signal of the operational amplifying means;

control means for selectively turning on and off the pull-up means and the pull-down means, respectively.

16. The amplifying apparatus of claim 15, wherein the control means is operable to control each of the pull-up and pull-down transistors, respectively, to be turned on for one of the following: less than about 1/2 of the period of a polarity signal; or less than the period of an output enable signal.

17. The amplifying circuit of claim 16, wherein the control means is operable to control each of the pull-up and pull-down transistors, respectively, to be turned on for one of the following: less than about 1/20 period of the polarity signal; or less than about 1/10 of the period of the output enable signal.

18. The amplifying circuit of claim 17, wherein the control means is operable to control each of the pull-up and pull-down transistors, respectively, to be turned on for one of the following: less than about 1/200 of the period of the polarity signal; or less than about 1/100 of the period of the output enable signal.

19. The amplifying apparatus of claim 15, wherein the control apparatus includes:

first one-shot means for providing a first one-shot signal that determines a duration that the pull-up means is turned on; and

second one-shot means for providing a second one-shot signal that determines a duration that the pull-down means is turned on.

20. The amplifying apparatus of claim 19, wherein the first and second one-shot signals are based upon an output enable signal.

21. The amplifying apparatus of claim 19, wherein each of the first and second one-shot means includes at least one delay means, respectively, to delay turning of the respective one-shot means relative to a transition in the output enable signal.

22. The amplifying apparatus of claim 15, wherein the operational amplifying means includes high-part means and low-part means, the pull-up means being operable to pull-up the output of the high-part means and the pull-down means being operable to pull-down the output of the low-part means.

23. The amplifying apparatus of claim 15, wherein the control means is further operable for selectively controlling the pull-up and pull-down transistors, respectively, based upon an output enable signal.

24. A liquid crystal display (LCD) device comprising:

an LCD panel; and

a plurality of source drivers connected to the panel;

each of the source drivers including an output buffer;

each output buffer including:

an operational amplifier;

a pull-up transistor connected to the output of the operational amplifier;

a pull-down transistor to the output of the operational amplifier;

a control circuit to selectively actuate the pull-up transistor and the pull-down transistor, respectively.

25. The LCD device of claim 24, wherein the control circuit is operable to selectively actuate each of the pull-up and pull-down transistors, respectively, for one of the following:

less than about 1/2 of the period of a polarity signal;

less than the period of an output enable signal;

less than about 1/20 period of the polarity signal;

less than about 1/10 of the period of the output enable signal;

less than about 1/200 of the period of the polarity signal; or less than about 1/100 of the period of the output enable signal.

26. The LCD device of claim 25, wherein the control circuit includes:

a first one-shot circuit to generate a first one-shot signal that determines actuation time of the pull-up transistor; and

a second one-shot rising circuit to generate a second one-shot signal that determines actuation time of the pull-down transistor;

the first and second one-shot signals being determined as a function of the output enable signal.

27. The LCD device of claim 26, wherein each of the first and second one-shot circuits includes at least one delay unit, respectively, to delay a transition in the respective one-shot signal relative to a transition in an output enable signal.

28. The LCD device of claim 25, wherein the operational amplifier includes a high-part amplifying sub-circuit and a low-part amplifying sub-circuit, the pull-up transistor being connected to the output of the high-part amplifying sub-circuit and the pull-down transistor being connected to the output of the low-part amplifying sub-circuit.

29. The LCD device of claim 25, wherein the control circuit is operable to selectively control the pull-up and pull-down transistors, respectively, based upon an output enable signal.